



### Features

- Lead free device (RoHS compliant\*)
- Protects up to 4 I/O ports
- Unidirectional configuration
- ESD protection
- Low capacitance 3 pF

### Applications

- Ethernet – 10/100/1000 Base T
- Personal digital assistant
- Handheld electronics
- Cellular phones
- Video cards

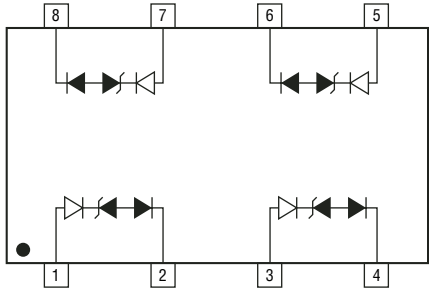
## CDNBS08-SLVU2.8-4 – Low Capacitance TVS Array

### General Information

The markets of portable communications, computing and video equipment are challenging the semiconductor industry to develop increasingly smaller electronic components.

Bourns offers Transient Voltage Suppressor Array combination diodes for surge and ESD protection applications in an 8 Lead Narrow Body SOIC package size format. Bourns Chip Diodes conform to JEDEC standards, are easy to handle on standard pick and place equipment and their flat configuration minimizes roll away.

The Bourns device® will meet IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (Surge) requirements.



### Electrical Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Peak Pulse Current (t <sub>p</sub> = 8/20 μs)	I <sub>PP</sub>		30		A
Peak Pulse Power (t <sub>p</sub> = 8/20 μs) <sup>1</sup>	P <sub>PP</sub>		600		W
Working Voltage	V <sub>WM</sub>			2.8	V
Breakdown Voltage @ 1 mA	V <sub>BR</sub>	3.0			V
Leakage Current @ V <sub>WM</sub>	I <sub>D</sub>			1.0	μA
Capacitance @ 0 V, 1 MHz	C		6		pF
Snapback Voltage		2.8			V
Clamping Voltage	@ I <sub>PP</sub> = 2 A	V <sub>C</sub>		5.5	V
	@ I <sub>PP</sub> = 5 A	V <sub>C</sub>		8.5	V
	@ I <sub>PP</sub> = 24 A	V <sub>C</sub>		15	V
	@ I <sub>PP</sub> = 30 A	V <sub>C</sub>		21	V

Note:  
1. See Peak Pulse Power vs. Pulse Time.

### Thermal Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Operating Temperature	T <sub>J</sub>	-55	+25	+150	°C
Storage Temperature	T <sub>STG</sub>	-55	+25	+150	°C

\*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.  
Specifications are subject to change without notice.  
Customers should verify actual device performance in their specific applications.

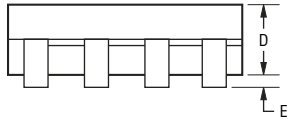
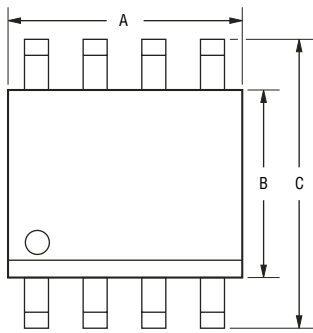
# CDNBS08-SLVU2.8-4 – Low Capacitance TVS Array



## Mechanical Characteristics

This is a molded JEDEC Narrow Body SO-8 package with lead free 100 % Sn plating on the lead frame. It weighs approximately 15 mg and has a flammability rating of UL 94V-0.

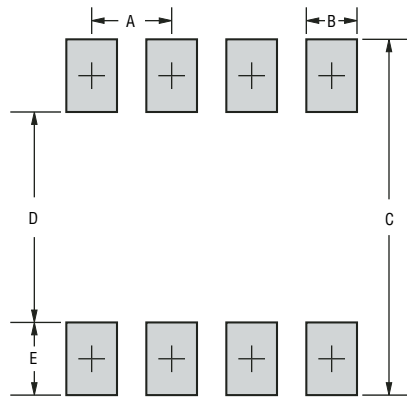
## Product Dimensions



DIMENSIONS =  $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

Dimensions	
A	$\frac{4.80 - 5.00}{(0.189 - 0.196)}$
B	$\frac{3.80 - 4.00}{(0.150 - 0.157)}$
C	$\frac{5.80 - 6.20}{(0.229 - 0.244)}$
D	$\frac{1.35 - 1.75}{(0.054 - 0.068)}$
E	$\frac{0.10 - 0.25}{(0.004 - 0.008)}$
F	$\frac{0.25 - 0.50}{(0.010 - 0.019)}$
G	$\frac{0.40 - 1.250}{(0.016 - 0.049)}$
H	$\frac{0.18 - 0.25}{(0.007 - 0.009)}$

## Recommended Footprint



Dimensions	
A	$\frac{1.143 - 1.397}{(0.045 - 0.055)}$
B	$\frac{0.635 - 0.889}{(0.025 - 0.035)}$
C	$\frac{6.223}{(0.245)} \text{ Min.}$
D	$\frac{3.937 - 4.191}{(0.155 - 0.165)}$
E	$\frac{1.016 - 1.27}{(0.040 - 0.050)}$

## How To Order

Common Code \_\_\_\_\_ **CD NBS08 - SLVU 2.8 - 4**

CD = Chip Diode

Package \_\_\_\_\_

NBS08 = Narrow Body SOIC8 Package

Model \_\_\_\_\_

SLVU = Low Capacitance TVS Array

Working Peak Reverse Voltage \_\_\_\_\_

2.8 = 2.8  $V_{RWM}$  (Volts)

Number of Diodes \_\_\_\_\_

## Typical Part Marking

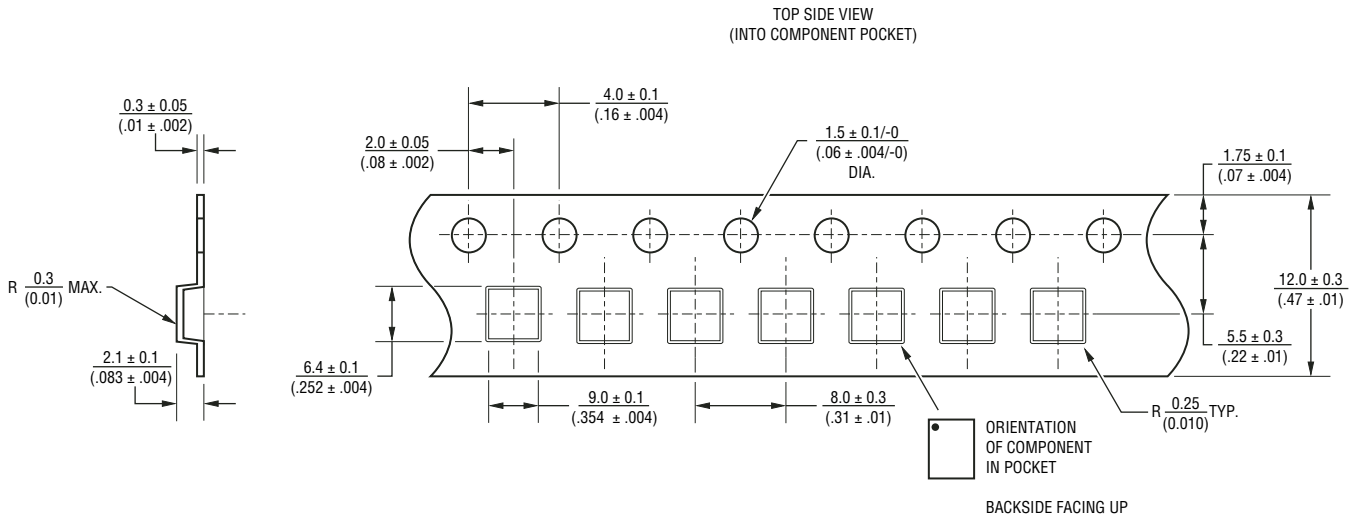
CDNBS08-SLVU2.8-4 ..... **SL4**

# CDNBS08-SLVU2.8-4 – Low Capacitance TVS Array

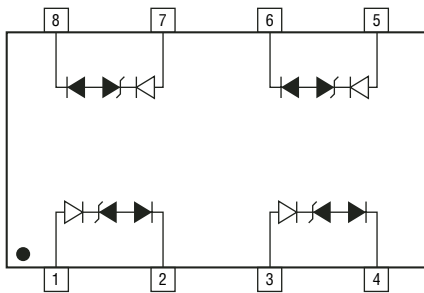


## Packaging

The surface mount product is packaged in a 8 mm x 4 mm Tape and Reel format per EIA-481 standard.



## Block Diagram

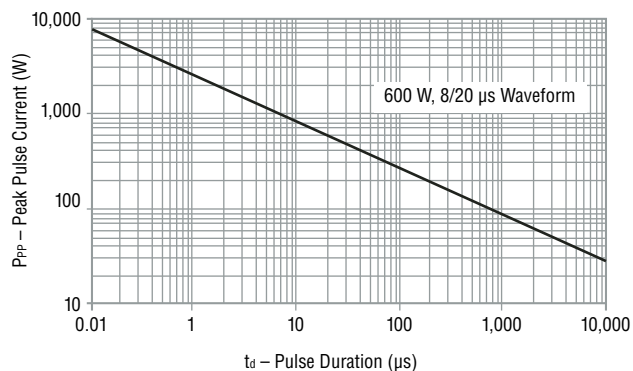


## Device Pinout

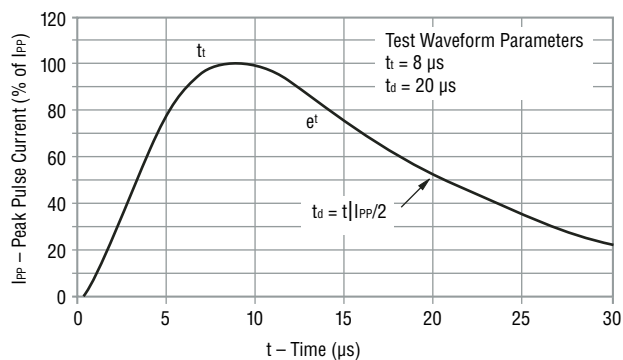
Pin	Unidirectional Common Mode	Bidirectional Common Mode	Bidirectional Differential Mode
1	Line 1	Line 1	Line Pair 1
2	GND	GND	Line Pair 1
3	Line 3	GND	Line Pair 2
4	GND	Line 2	Line Pair 2
5	Line 4	Line 2	Line Pair 2
6	GND	GND	Line Pair 2
7	Line 2	GND	Line Pair 1
8	GND	Line 1	Line Pair 1

Performance Graphs

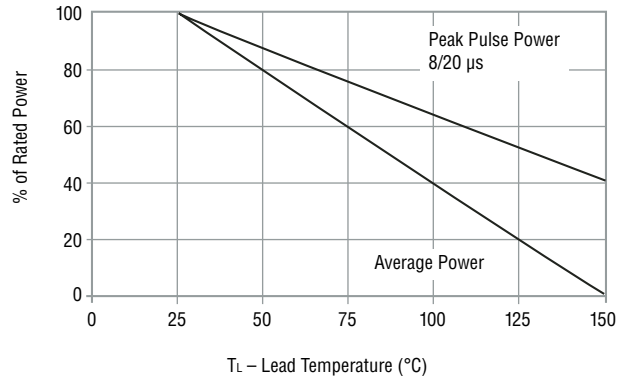
Peak Pulse Power vs Pulse Time



Pulse Wave Form



Power Derating Curve



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